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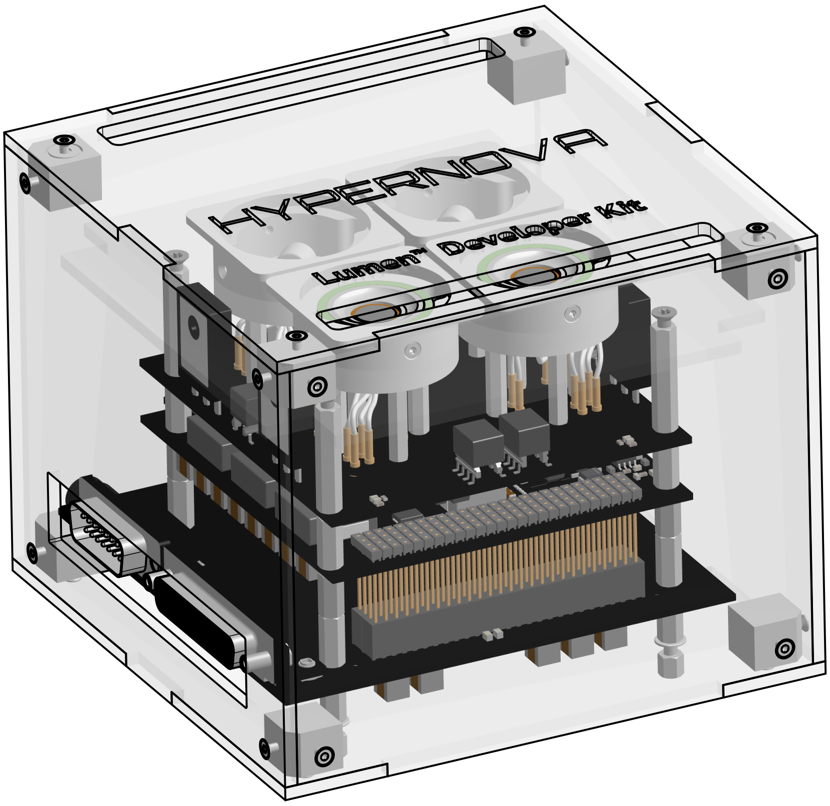

Lumen™ Developer Kit [V1.0]

Interface Control Document (ICD)

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Controlled document note: It is the user's responsibility to verify that the version of any printed documentation matches the configuration-controlled version.

Document Information

I. Reviewer(s)

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3		

II. Document History

Revision	Date	Change details	Sections
0.1	2023-07-27	Initial draft	All

III. Acronyms, Abbreviations and Symbols

The ECSS glossary of terms (ECSS-S-ST-00-01) is used as the normative reference for this document. The table below intends to add to or highlight the terms described in ECSS S-ST-00-01.

Term	Description
DOC	Document

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1 INTRODUCTION

The Lumen™ Developer Kit [Version 1.0] (otherwise referred to as "the Kit") is a modular benchtop system for delivering pulsed plasma jets in a controlled and precise manner. The Kit layout described in this document is for the standard configuration containing a total of four (4) thrusters located on top of the Kit PCB boards.

One pair of thrusters is configured in *"Dummy Mode"*, where the pulses are discharged through a surge arrestor. The discharge lights up the arrestor for visual aid. *Dummy Mode* is most suitable for non-destructive operation & long-term test firings.

The second pair of thrusters is configured in *"Hot Mode"*, where the pulses are discharged through air-gapped thrusters. The discharge creates an exposed plasma arc into the ambient air, which is loud and bright. *Hot Mode* is the closest representation of plasma jet creation in a non-vacuum environment, but eventually wears out the thruster components due to erosion.

2 DOCUMENTS

2.1 Applicable Documents

The following documents are applicable and are referred to as [ADxx] in the text. Documents are applicable in their entirety. For unspecified issues of document, the latest signed version should be used. For specified issues, subsequent amendments to or revisions of any of these publications do not apply. However, parties to the agreement based on this document are encouraged to investigate the possibility of applying the most recent issue.

Table 2-1: Applicable Documents

Reference	Document Number	Issue/Date	Title
AD01			
AD02			

2.2 Reference Documents

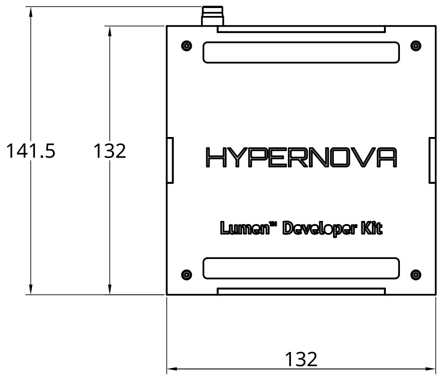
The following documents are referenced for supporting information only and are referred to as [RDxx] in the text. For unspecified issues of a document, the latest issue should be used. Any sections that are applicable will be referenced directly in the requirements section of this technical specification.

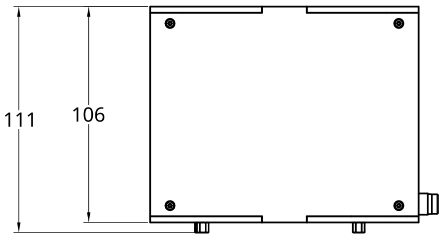
Table 2-2: Reference Documents

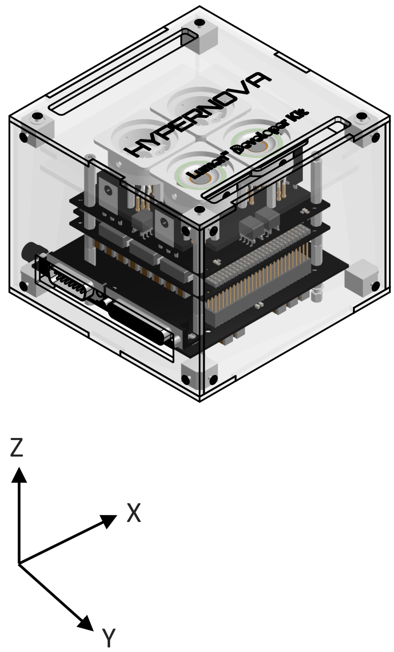
Reference	Document Number	Issue/Date	Title
RD01			
RD02			

3 GEOMETRIC AND MASS PROPERTIES

The Kit internals (PCB boards & thrusters) occupies the equivalent volume of a 0.5U CubeSat. Figure 3-1 and Figure 3-2 below display the overall dimensions and Centre of Mass location of the Kit (both with and without the safety enclosure). The total nominal mass of the Kit is 867 g and 427 g, with and without the safety enclosure respectively.







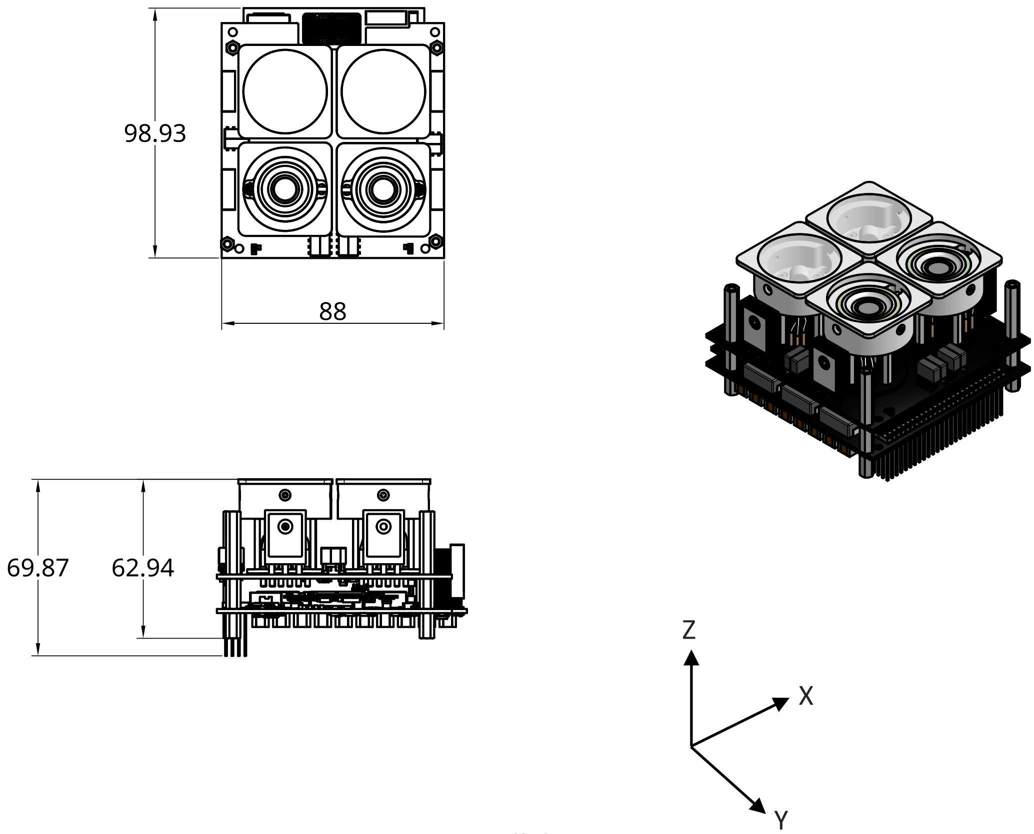


Figure 3-1: Overall dimensions

Figure 3-2 below displays the Kit Centre of Mass (CoM):

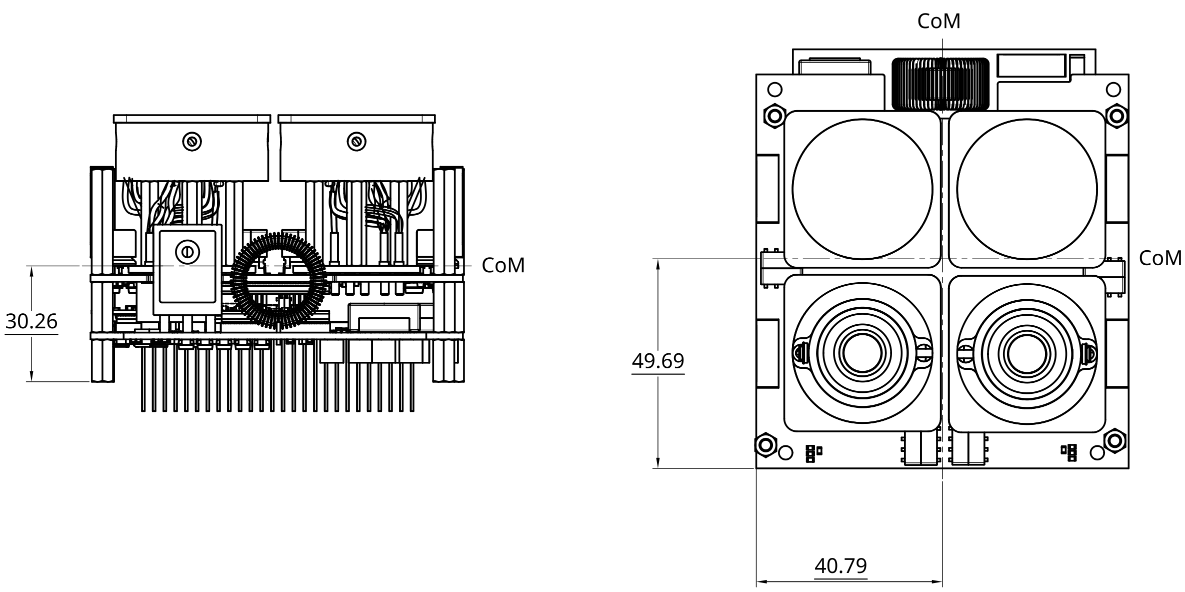


Figure 3-2: Kit CoM

Mass Moment of Inertia:

Ixx = 4.2E5 g/mm^2
Iyy = 4.2E5 g/mm^2
Izz = 5.8E6 g/mm^2

4 MOUNTING INTERFACE

The Kit is mounted to the safety enclosure via four (4) M3 fastener holes (3.2 mm diameter clearance) through the Kit boards along the Z-axis as shown in Figure 4-1 below. Threaded hex spacers are installed for structural rigidity. The mounting footprint conforms to the standard CubeSat PC104 form factor.

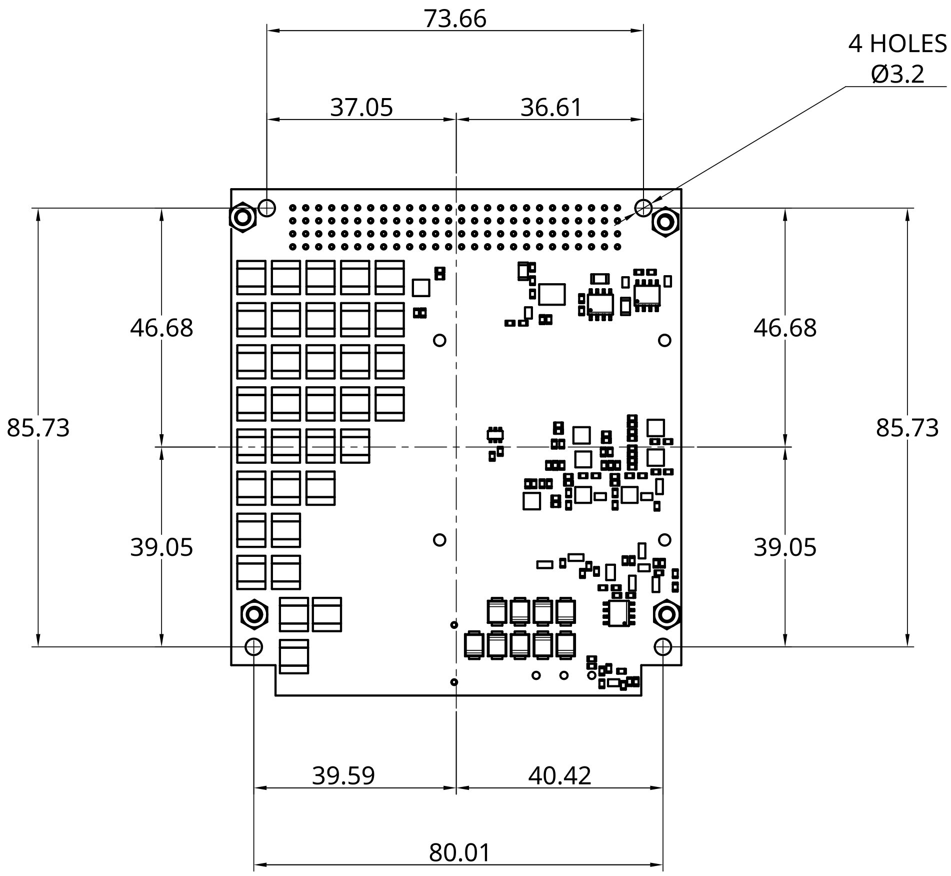


Figure 4-1: Mounting Interface

5 THERMAL

Operating temperature range: -20°C to +50°C
Survival temperature range: -40°C to +80°C

6 SAFETY ENCLOSURE

The Kit is housed in a plastic enclosure for user safety. The top lids are removeable to swap out the thrusters as desired shown in Figure 6-1. With some effort, it is also possible to remove the Kit from the enclosure which can be seen in Figure 6-2.

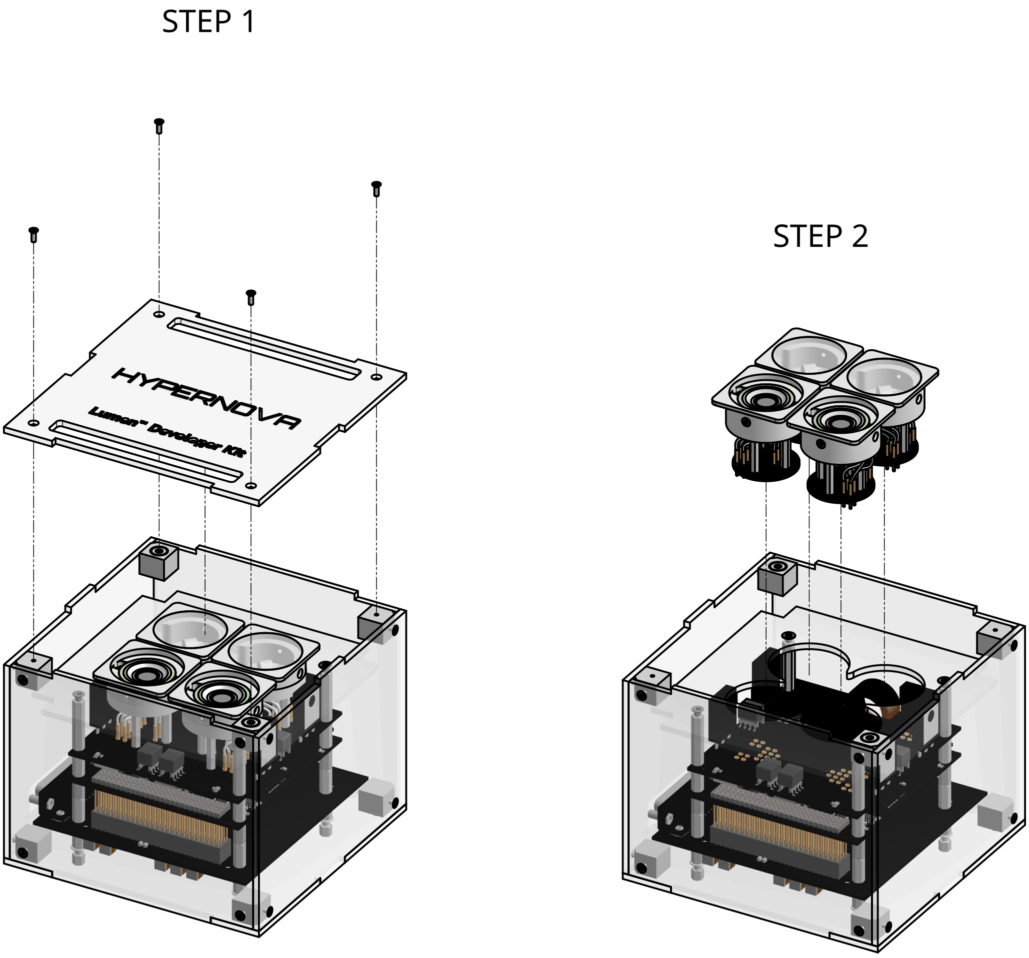


Figure 6-1: Removal of the Thruster Heads

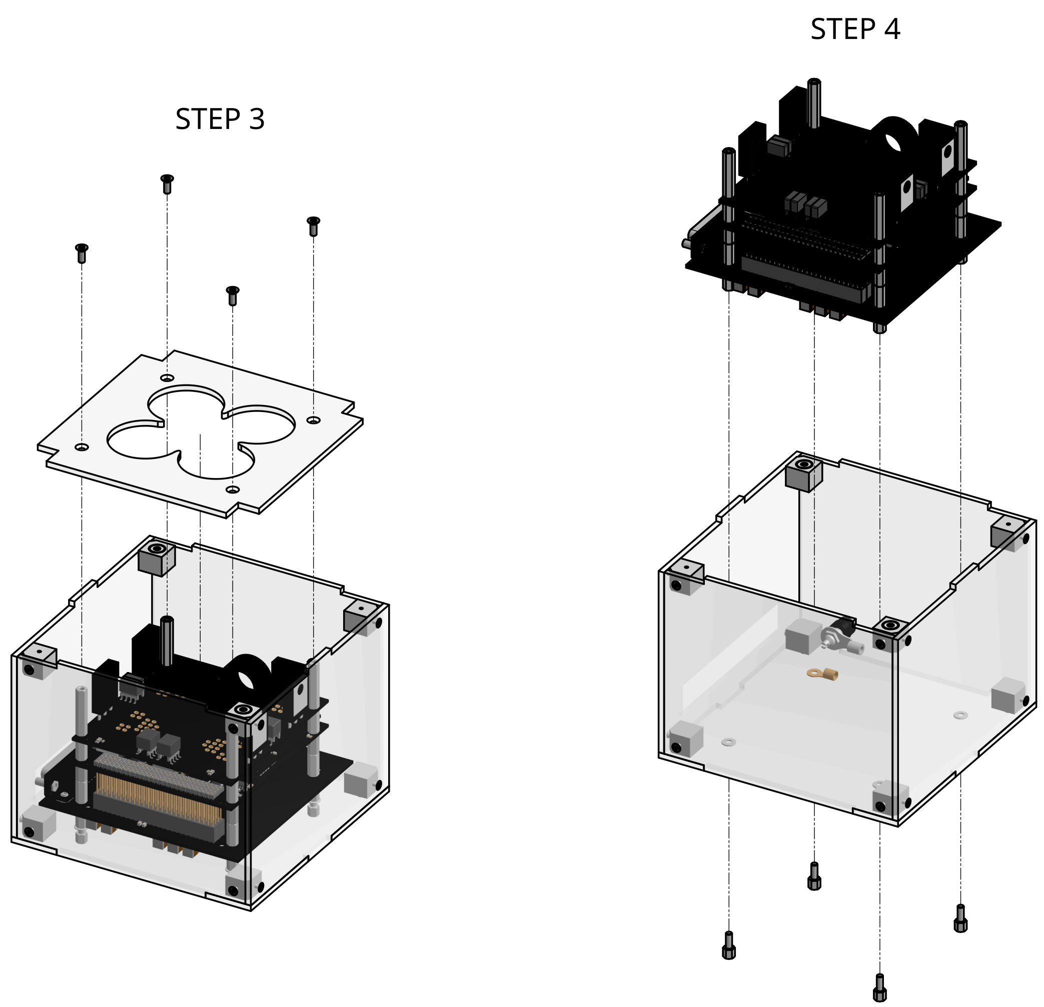


Figure 6-2: Removal of the entire Lumen ™ Kit

7 PLUME CONSIDERATIONS

The thruster plume consists of discharge plasma. Avoid touching or placing foreign objects near the exposed thruster heads of the Kit. A minimum keep-out zone of ±90 degrees about the normal direction of the thruster head front face and several cm's radial distance is advised as illustrated in Figure 7-1 below.

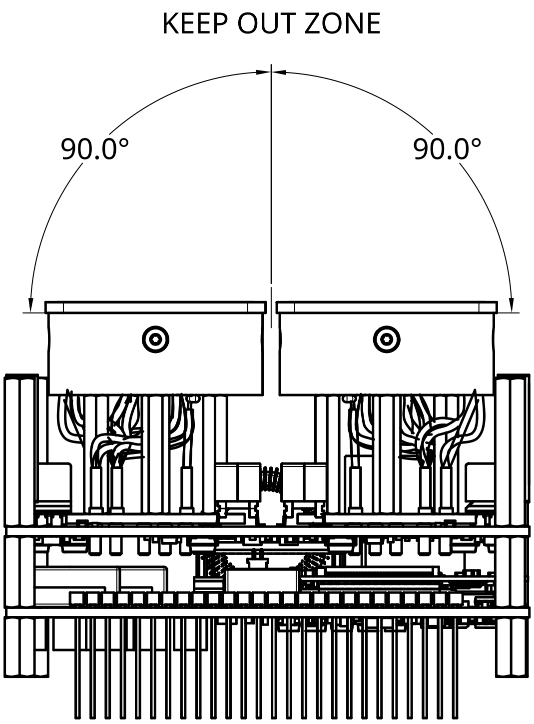


Figure 7-1: Keep out zone for thruster head plume

8 ELECTRICAL INTERFACE

8.1 PC104 Header Connectors H1 and H2: Main System Interface

8.1.1 Overview

The Kit conform to the PC104 form factor[1] which includes two side-by-side header connectors, H1 and H2. These connectors are used to supply power to the Kit and communication interfaces to the rest of the system. Figure 8-1 below shows a CAD drawing of the connectors on the GSE board.

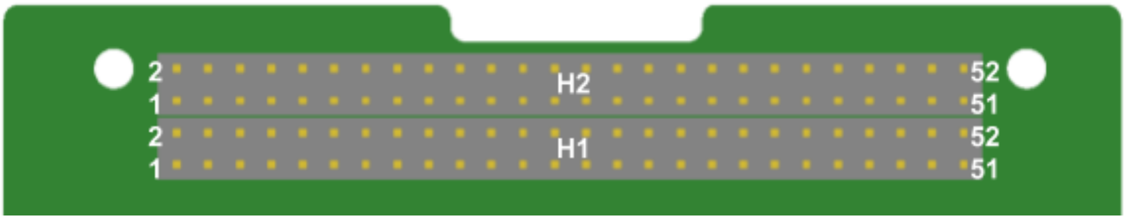


Figure 8-1: CAD Drawing Showing the Top View of Connectors H1 and H2

8.1.2 Part Information

Table 8-1 below gives the part information for connectors H1 and H2.

Table 8-1: Part information for connectors H1 and H2

Parameter	Specification
Type	PC/104 connector
Number of Contacts	2 rows × 26
Gender	Female
Manufacturer	Samtec
Manufacturer Part Number	SSQ-126-03-G-D

Figure 8-2 and Figure 8-3 below show the mechanical drawings of the connector:

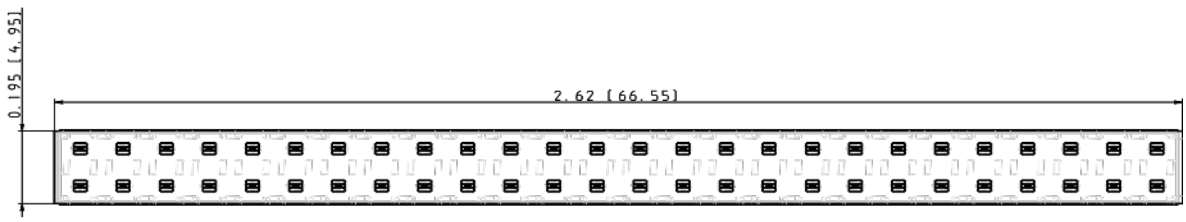


Figure 8-2: Top View of Samtec Connector SSQ-126-03

[1] https://pc104.org/wp-content/uploads/2015/02/PC104_Spec_v2_6.pdf

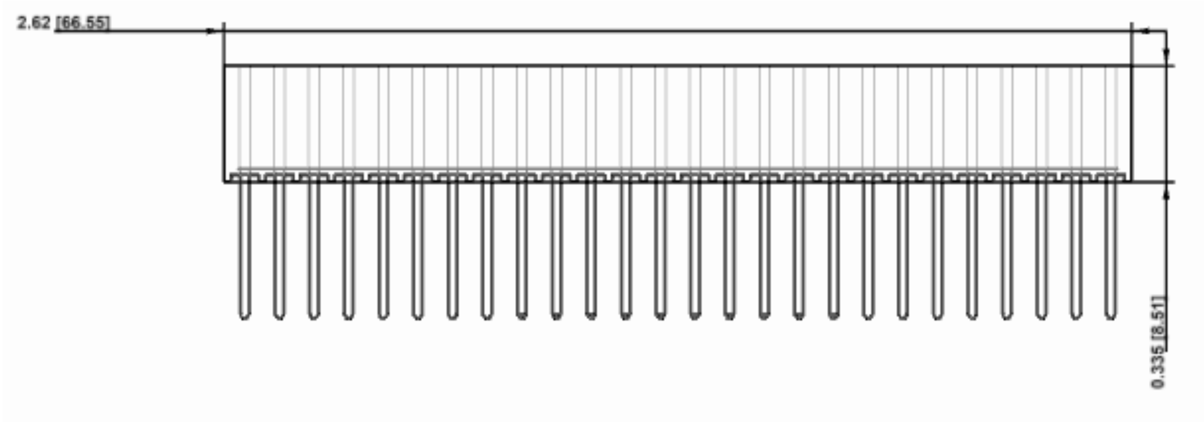


Figure 8-3: Front View of Samtec Connector SSQ-126-03-G-D

8.1.3 Pinout

Figure 8-4 below shows the pin numbering for connector H1 and H2:

H2	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52
	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51
H1	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52
	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51

Figure 8-4: Pinout for connectors H1 and H2 (top view)

8.1.4 Pin Description

Table 8-2 and Table 8-3 below provide the pin allocations for connectors H1 and H2, respectively.

Table 8-2: Pin allocations for connector H1

Description:	H1		Description:
–	1	2	–
–	3	4	–
–	5	6	–
–	7	8	–
–	9	10	–
–	11	12	–
–	13	14	–
–	15	16	–
Secondary RS-485 B	17	18	Secondary RS-485 A
–	19	20	–
– *[optional: Primary I2C SCL]*	21	22	–
– *[optional: Primary I2C SDA]*	23	24	–
–	25	26	–
–	27	28	–
–	29	30	–
–	31	32	–

–	33	34	Primary RS-485 B
–	35	36	Primary RS-485 A
–	37	38	–
–	39	40	–
– *[optional: Secondary I2C SDA]*	41	42	–
– *[optional: Secondary I2C SCL]*	43	44	–
–	45	46	–
–	47	48	–
	49	50	
5V Power Supply	51	52	3.3V Power Supply

Table 8-3: Pin allocations for connector H2

Description:	H2		Description:
–	1	2	–
–	3	4	–
–	5	6	–
–	7	8	–
–	9	10	–
–	11	12	–
–	13	14	–
–	15	16	–
–	17	18	–
–	19	20	–
–	21	22	–
12V Power Supply	23	24	12V Power Supply
– *[optional: Alternate 5V Power Supply]*	25	26	– *[optional: Alternate 5V Power Supply]*
– *[optional: Alternate 3.3V Power Supply]*	27	28	– *[optional: Alternate 3.3V Power Supply]*
GND	29	30	GND
GND	31	32	GND
–	33	34	–
–	35	36	–
–	37	38	–
–	39	40	–
–	41	42	–
–	43	44	–
Battery “Raw” Bus	45	46	Battery “Raw” Bus
– *[optional: Primary SPI MISO]*	47	48	- *[optional: Primary SPI MOSI]*
UART, OBC Tx *[optional: Primary SPI SCLK]*	49	50	UART, OBC Rx *[optional: Primary SPI nSS]*
–	51	52	–

8.1.5 Power Ground

All signals are referred to (power) ground [GND]. Power ground is isolated from the Kit's PCB boards by at least 1GΩ at 100V.

On the safety enclosure, Hex spacer extension feet are provided for grounding to an ESD mat. An additional grounding option in the form of a banana socket connector is also provided on the side panel of the enclosure.

8.1.6 Power Supply

Table 8-4 details the power supply requirements of the Kit:

Table 8-4: Power Supply Requirements

Parameter	Nominal	Range
3.3V Power Supply Voltage	+3.30V	+3.14V / +3.46V
5V Power Supply Voltage	+5.00V	+4.75V / +5.25V
12V Power Supply Voltage	+12.00V	+11.4V / +12.6V
3.3V Power Supply Current	120mA	200 mA
5V Power Supply Current	70mA	150 mA
12V Power Supply Current	10mA	< 4000mA

Depending on the mode of operation, the Kit may draw peak power of between 1 and 20W directly from the 12V supply.

8.1.7 Overcurrent Protection

No over-current protection is provided on the input power rails on the Kit itself. It is expected the over-current protection is provided by the power supply or Satellite EPS. The Kit does however provide telemetry feedback for the current consumption which could be used by the system to detect a problem. There is also trip circuitry to protect some of the critical power components. The trip status can be read via telemetry and reset with a telecommand.

8.1.8 Inrush Current

A current limiting circuit limits the current to a maximum of 4A on the 12V supply. The maximum inrush current on the 5V and 3.3V supplies is 500mA for 100ms [TBC] after power on.

8.1.9 Communication Interfaces

The Kit is configured to operate via the UART communication interface by default. Alternative interfaces for the Kit are described below.

8.1.9.1 RS-485 (optional)

Table 8-5 details the electrical specification of the RS485 communications interface.

Table 8-5: RS-485 electrical specifications

Parameter	Specification
Network Topology	Point-to-point or Multi-dropped
Signal Type	Differential Input / Output
Input Differential Threshold	± 0.2V
Mark (1)	Negative Voltages
Space (0)	Positive voltages
Operational Differential Voltage Range	−10V to +10V
Operational Common Mode Voltage Range	−7V to +7V
Termination	Open

8.1.9.2 I2C Bus (optional)

Table 8-6 details the electrical specification of the I2C communications interface.

Table 8-6: I2C electrical specifications

Parameter	Specification
Network Topology	Point-to-point or Multi-dropped
Signal Type	Single-ended open collector
Onboard pull-up resistor	10kΩ to 5V
Output Low current-sink	10mA
Maximum input voltage	5.25V

8.1.9.3 SPI Bus (optional)

Table 8-7 details the electrical specification of the SPI bus communications interface.

Table 8-7: SPI Bus electrical specifications

Parameter	Specification
Network Topology	Point-to-point
Signal Type	LVCMOS
Onboard pull-up resistor	None
High-level input voltage	2.0V
Low-level input voltage	0.8V
Maximum input voltage	5.5V
Maximum output voltage	3.3V
Output Low current-sink	20mA
Output High current-source	20mA

9 SOFTWARE INTERFACE

Communication with the Kit occurs through either the RS485, I2C, UART or SPI communications interfaces. Primary and secondary RS485 and I2C interfaces are provided. As there are no secondary SPI or UART interfaces. All the communications interfaces access the same internal registers of the Kit and thus have equivalent functionality. If required, multiple communications interfaces can be used simultaneously as the Kit has internal bus-arbitration to handle simultaneous read/writes to the same registers. In the case of I2C, SPI, UART and RS485, the Kit is a slave on the bus. Communication occurs through the issuing of a telecommands and telemetry requests. In the case of a telecommand, the Kit responds with an ACK, or NAK if the telecommand was invalid. In the case a telemetry request, the Kit response with associated data, or a NAK if the telemetry request was invalid.

9.1 RS485 / UART

The Kit has a powerful 166-MHz 32-Bit ARM Cortex-M3 processor with multiple UART peripherals. The UART peripherals on the processor are connected to separate RS485 driver chips to create a primary and a secondary RS485 bus. The processor can implement almost any serial protocol depending on the platform specific requirements, but the default implementation is described below. The default UART configuration is given in Table 9-1:

Table 9-1: Default UART Configuration Parameters

Parameter	Specification
Baud Rate	115 200
Data Bits	8
Parity	None
Stop Bits	1

SLIP framing is used to frame data packets. Messages are transmitted using the Nanosatellite Protocol (NSP). NSP messages are composed of five data fields as shown in Table 9-2 below:

Table 9-2: NSP Message Fields

Destination Address	Source Address	Message Control	Message Data	Message CRC
(1 byte)	(1 byte)	(1 byte)	(0 to 256 bytes)	(2 bytes)

The length of an NSP message is therefore five plus the number of Message Data bytes. The Message Control byte consists of 5 command bits, an acknowledge bit, a package correlation bit and reply bit. CRC-16-CCITT is used for the CRC calculation which has a polynomial of $x^{16}+x^{12}+x^5+1$ (0x1021). For data type larger that a byte, e.g. 32-bit integers, least significant bytes are transmitted first i.e. little-endian format.

9.2 I2C (optional)

The I2C bus consists of two signals namely SCL and SDA. SCL is the clock signal, and SDA is the data signal. I2C bus drivers are open drain, meaning that they pull the signal lines low, but cannot drive high. This ensures that there can never be bus contention that could cause damage to one the drivers. Both signal lines have a pull-up resistor that restores the signal to high when no device is asserting it low.

The Kit acts as an I2C slave node with 7-bit addressing. The slave address of the Kit pre-configurable. Figure 9-1 below shows the basic protocol used in I2C.

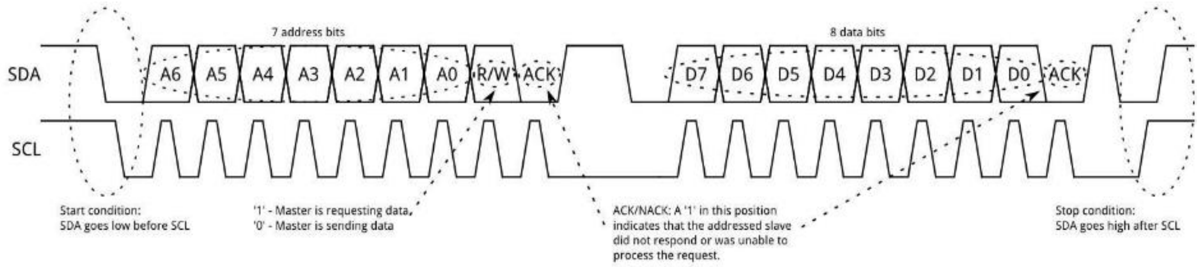


Figure 9-1: Basic I2C Timing Diagram

In the case of a telecommand to the Kit, the master will issue an I2C write command, i.e. R/W bit = ‘0’, the I2C first data byte will contain the address of the telecommand, and the subsequent I2C data bytes (up to 256) should contain the telecommand data payload.

In the case of a telemetry request to the Kit, the master will issue an I2C write command, i.e. R/W bit = ‘0’, where I2C first data byte will contain the telemetry request address. Immediately following this, the I2C master should issue a I2C read request, i.e. R/W bit = ‘1’ to read the telemetry response.

9.3 SPI (Optional)

The SPI bus consists for 4 signals namely:

1. SCLK: Serial Clock output from master
2. MOSI: Master-Out Slave-In
3. MISO: Master-In Slave-Out
4. SS: active low Slave Select output from master.

Because SPI is a synchronous data communications interface with push-pull drivers, it can generally support mush greater speeds that RS422 or I2C over short distances e.g. 1Mbps board-to-board, and 20Mbps directly between ICs. Figure 9-2 below shows the general connection diagram of SPI signals between two devices.

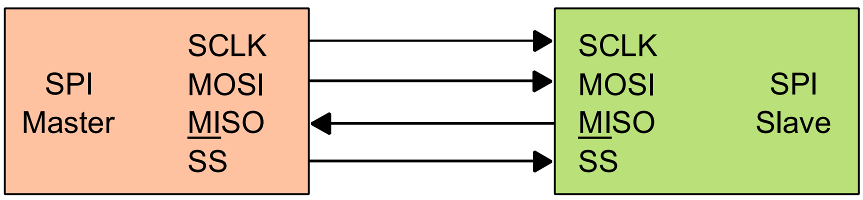


Figure 9-2: Basic SPI connection diagram

Figure 9-3 below shows the basic timing diagram for SPI signals. The Kit uses SPI mode 0 (CPOL=0, CPHA=0) in which data is sampled on the rising edge of the clock pulse and shifted on the falling edge of the clock pulse.

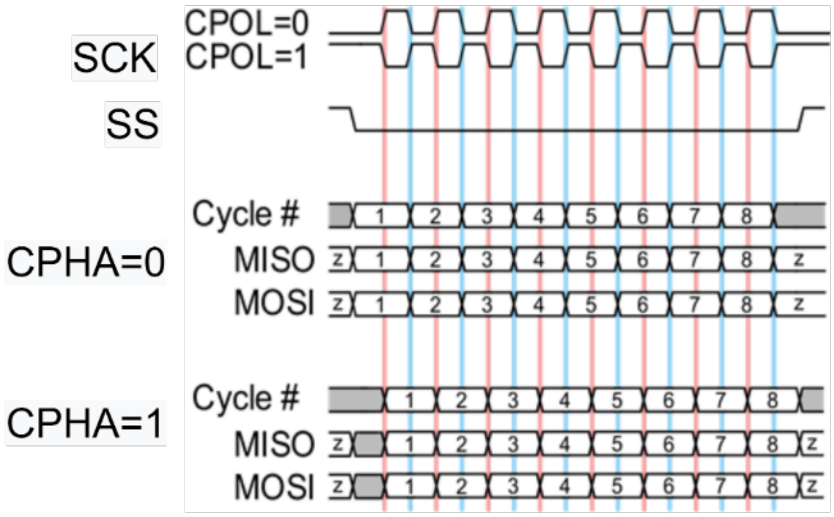


Figure 9-3: Basic timing diagram for SPI signals

In the case of a telecommand to the Kit, the first data bit sent from the master should be low (indicating a write command), the next 7 bits from the master should contain the address of the telecommand, and the data bytes (up to 256) following should contain the telecommand data payload.

In the case of a telemetry request to the Kit, the first data bit sent from the master should be low (indicating a read command), the next 7 bits from the master should contain the address of the telemetry request. Subsequent data clocked out from the slave in the same SPI transaction will contain the telemetry data payload.

9.4 CAN Bus (optional)

The Kit makes provision for a CAN bus interface, which can be routed to the header connector if required. The CAN bus has many years of heritage in automotive and industrial applications and is also qualified for space use. The Kit conforms to ISO 11898-2, thus supporting bit speeds up to 1 Mbit/s. The Kit supports the extended frame format according to CAN 2.0 B. The Kit implements the CAN bus extension protocol described in ECSS-E-ST-50-15C (http://ecss.nl/standard/ecss-e-st-50-15c-space-engineering-canbus-extension-protocol-1-may-2015/)

9.5 Telecommands and telemetries

Telecommands and telemetry available in the Kit are given in Table 9-3 and Table 9-4 respectively.

Table 9-3: List of Telecommands

Address	Description
0x00	Software Reset. Initiates a software reset of the FPGA fabric..
0x01	Set UTC Time. The time is Unix format.
0x02	Set Trigger Source. Selects the trigger source for initiating a firing sequence. Possible sources are (i) immediate software trigger, (ii) UTC time match, (iii) external discrete trigger.
0x03	Upload Trigger Table. The trigger table contains 256 entries where each entry contains the thruster selection and a dwell time in ms.

0x04	Set Trigger Table Config. Sets the start and stop pointers to entries in the trigger table, and a loop counter that indicates the number of times the Kit should repeat the trigger sequence.
0x05	Upload Switch Table. The switch table contains 256 entries where each entry contains the state of the switches on the PPU, as well as the dwell time in µs.
0x06	Set Switch Table Config. Sets the start and stop pointers to entries in the switch table. The Kit will execute the selected sequence each time a trigger is generated.
0x07	Start Firing Sequence. Generates an immediate software trigger that starts the firing sequence configured using the Set Trigger Table Config telecommand (0x04).
0x08	Stop firing Sequence. Immediately halts the any firing sequence currently executing.
0x09	Set PPU Config. Resets over-current flags, enable/disable the DC-DC converter and sets the DC-DC converter setpoint voltage.
0x0A	Set Measurement Config. Used to clear the raw and stats FIFOs, set the pulse detection threshold and the thruster filter selection for storing raw data samples.

Table 9-4: List of Telemetry

Address	Description
0x80	Get Part Number.
0x81	Get Serial Number
0x82	Get Version Info.
0x83	Get Device Info
0x84	Get Runtime
0x85	Get UTC Time
0x86	Get Onboard Telemetry. Reads the internal voltages, currents and temperatures.
0x87	Get Trigger Status. Reads the trigger controller busy flag, current pointer, and remaining loops.
0x88	Get Switch Status. Reads the switch controller busy flag and current pointer.
0x89	Get PPU Status. Reads the over-current flags and DC-to-DC voltage.
0x90	Get Measurement Status. Reads the measurement controller busy flag, raw and stats FIFOs used words.
0x91	Read Raw Data FIFO. Read raw voltage and current samples from the raw data FIFO.
0x92	Read Stats FIFO. Read the output voltage and current statistics FIFO.
0x93	Get Trigger Counters. Read the number of times each thruster has been fired.
0x94	Get Persistent Trigger Counters